Substitute for form 1449/PTO Modified	*Complete if Known*	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)* Sheet of	Application Number	10/726,902
	Confirmation No.:	4177
	Filing Date:	December 3, 2003
	First Named Inventor:	Mitchell Alsup
	Art Unit:	2183
	Examiner Name:	Fennema, Robert E
	Attorney Docket Number:	5500-88700

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
RF		US-5,381,533	1/10/95	Peleg, et al.	
		US-			
		US-			
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FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code-Number-Kind Code *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	Check if English Translation is attached
RF	A1	GB 2 381 101	4/23/03			☐
RF	A2	EP 0 957 428	11/17/99			☐

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, (page(s), volume-issue number(s), publisher, city and/or country where published.	Check if English Translation is attached
RF	A3	International Search Report and Written Opinion for PCT/US2004/039269, mailed December 12, 2005, 11 pages.	☐

Examiner Signature	/Robert Fennema/	Date Considered	08/17/2006

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*	Application Number	10/726,902
	Confirmation No.:	4177
	Filing Date:	December 3, 2003
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	Examiner Name:	Fennema, Robert E.
Sheet 1 of 2	Attorney Docket Number:	5500-88700

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number — Number-Kind.Code *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
RF		US-7,003,629	2/21/06	Alsup	
		US-6,449,714	9/10/02	Sinharoy	
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						☐
						☐

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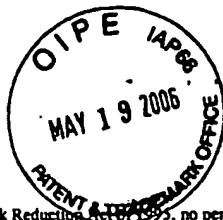
Substitute for form 1449/PTO Modified	Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)* Sheet 2 of 2	Application Number	10/726,902
	Confirmation No.:	4177
	Filing Date:	December 3, 2003
	First Named Inventor:	Mitchell Alsup
	Art Unit:	2183
	Examiner Name:	Fennema, Robert E.
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RF	A1	Yuan Chou, et al., "Instruction Path Coprocessors," March 2000, pp. 1-24.	☐
	A2	Friendly, et al., "Putting the Fill Unit to Work: Dynamic Organizations for Trace Cache Microprocessors," Dept. of Electrical Engineering and Computer Sciences, The Univ. of Michigan, December 1998, 9 pages.	☐
	A3	Bryan Black, et al., "Turboscalar: A High Frequency High IPC Microarchitecture," Dept. of Electrical and Computer Engineering, Carnegie Mellon Univ., June 2000, pp. 1-	☐
	A4	Merten, et al., "An Architectural Framework for Run-Time Optimization," June 2001, pp. 1-43.	☐
	A5	Jourdan, et al., "Increasing the Instruction-Level Parallelism through Data-Flow Manipulation," Intel, 11 pages.	☐
	A6	Hinton, G., et al., "A 0.18-MUM CMOS IA-32 Processor with a 4-GHZ Integer Execution Unit," IEEE Journal of Solid-State Circuits, Vol. 36, No. 11, November 2001, pages. 1617-1627.	☐
	A7	Sanjay J. Patel, et al., "replay: A Hardware Framework for Dynamic Optimization," IEEE, Vol. 50, No. 6, June 2001, pp. 590-608.	☐
	A8	Jacobson, et al., "Instruction Pre-Processing in Trace Processors," IEEE Xplore, January 1999, 6 pages.	☐
	A9	Bryan Black, et al., "The Block-Based Trace Cache," IEEE, 1999, pp. 196-207.	☐
	A10	Palmer, et al., "Fido: A Cache That Learns to Fetch," Proceedings of the 17th International Conference on Very Large Data Bases, Barcelona, September 1991, pp. 255-264.	☐
	A11	Chen et al., "Eviction Based Cache Placement for Storage Caches," USENIX 2003 Annual Technical Conference, (13 pages)	☐
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